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Docket No.: 60188-028

**PATENT**

JCE72 U.S. PTO  
09/779751  
02/09/01

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Application of

Toshio YAMADA

Serial No.:

(Divisional of Serial No. 09/102,166)

Group Art Unit:

Filed: February 09, 2001

Examiner:

For: SEMICONDUCTOR INTEGRATED CIRCUIT, COMPUTER SYSTEM, DATA  
PROCESSOR AND DATA PROCESSING METHOD

**INFORMATION DISCLOSURE STATEMENT**

Commissioner for Patents  
Washington, DC 20231

Dear Sir:

In accordance with the provisions of 37 C.F.R. 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached form PTO-1449. It is respectfully requested that the references be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.


This Information Disclosure Statement is being filed within three months of the U.S. filing date OR before the mailing date of a first Office Action on the merits. No certification or fee is required.

(Divisional of Serial No. 09/102,166)

The references were cited by or submitted to the U.S. Patent and Trademark Office in parent application Serial No. 09/102,166, filed June 22, 1998, which is relied upon for an earlier filing date under 35 USC 120. Thus, copies of these references are not attached. 37 CFR 1.98(d).

Respectfully submitted,

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